PDP-1 COMPUTER
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PDP-35-2

INSTRUCTION MANUAL

PART 3--IOT OPERATED I/O DEVICES

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3.1 Input/Output Transfer Instructions

On the original PDP-1 all input/output operations were done using iot instructions (op. code 72). Early timesharing systems were designed to be able to run non-TS programs with (almost) no changes. In present systems, the ivk instruction provides more general I/O capabilities (see part 5 of this instruction manual). This memo describes I/O devices which are still operated by iot instructions.

Some I/O devices must be assigned before they are used. This avoids conflicts since only the program which has a given I/O unit assigned can use that unit. An iot which references an unassigned device will be ignored.

The instruction mta 500 (770570) is used to assign and deassign external levels and the External Register. The action of the mta 500 is determined by the contents of A as follows.

A[0-5] Operation

00 Assign external levels. For all i, $1 \leq i \leq 7$, external level i is assigned if A[i+10] = 1.
For example, to assign external level 2,
A should contain 40.
The mta 500 will skip if the assignment is successful, i.e. no one else has the level(s) assigned.

01 Deassign external levels as above. No skip.

02 Assign External Register, shared. Skip if successful, i.e. no one else has it assigned as private.

03 Assign External Register, private. Skip if successful, i.e. no one else has it assigned.

04 Deassign External Register. No skip.

3.2.1 External Register

The PDP-1 External Register is an 18-bit register which can be loaded and read by the PDP-1 and by I/O devices. The music hardware, the TX-0 data link, and the 8-bit D→A converter use the External Register. The External Register must be assigned before it can be used.

Instruction	Action
lei (724577)	Load External Register from I.
lea (724677)	Load External Register from A.
rer (724777)	Read External Register into I.

3.2.3 Typewriter Input

The instruction tyi(720004) waits for a character to be typed on the typewriter. When a key is struck, the six-bit flexo code for the character is placed in I[12-17], and I[0-11] is cleared. If a character is typed before the tyi is executed, the tyi will read that character without waiting.

The type in status bit is set whenever a key is struck, and is cleared when a tyi is executed. It is read by bit 3 of the status word (see cks instruction). The status bit tells when there is a character to be read. The type in status bit will cause sequence breaks on channel 6 if it is enabled (see the section on sequence breaks).

3.2.4 Typewriter Output

The instruction tyo(730003) causes the character specified by the right six bits of I to be printed on the typewriter. The bits I[0-11] are ignored.

The type out status bit is cleared when a tyo is executed, and is set when the typewriter has finished printing the character. It is read by bit 2 of the status word (see cks instruction). The status bit is on whenever the typewriter is capable of accepting another character to be printed. The type out status bit will cause sequence breaks on channel 7 if it is enabled (see the section on sequence breaks).

3.2.5 CRT Display

The display is intended to be used as an on-line output device for the PDP-1. It is useful for high speed presentation of graphs, diagrams, drawings, and alphanumeric information. The unit uses solid-state circuits and has magnetic deflection and focus. The cathode ray tube has a P7 phospher, allowing either a blue or yellow filter to be used to select the short or long persistence for photography purposes. Some characteristics of the display are --

1024 by 1024 addressable locations
Plots 20,000 points per second
Random point plotting
Accuracy of point is 3 percent of raster size
Raster size is 9.25 by 9.25 inches
Origin may be at one of four points under control of each display instruction
Brightness may be controlled to one of 8 levels under control of each display instruction

To the unaided eye, approximately 512 points are resolvable on each axis. Five of the eight brightness levels are visible. A photomultiplier tube may see all brightness levels.

The dpy instruction (73cb07) causes one point to be displayed on the scope. A[0-9] specifies the X coordinate and I[0-9] gives the Y coordinate. A and I remain unchanged after the dpy instruction. The three "b" bits control the brightness -- 4 is visible to photomultiplier tubes only, 7 is barely visible in a dark room, 0 is normal, and 3 is brightest. The "c" bits control the centering. 0 makes the origin in the center of the scope. 1 puts it at the center of the bottom edge. 2 makes the origin be half way up the left edge, while 3 puts it at the lower left corner.

A dpy (that is with the i-bit on) takes 50 microseconds to complete. dpy-i (iot 7) does not wait for the scope to complete. Since it is impossible to activate the scope too fast, one normally executes iot 7 instructions. This allows the program to continue while the scope is running.

Subroutines for plotting points and lines exist in the FORTRAN library.

3.2.6 Light Pen

The light pen is designed to be used with the CRT display (see 3.2.5). By "writing" on the face of the CRT, stored or displayed information can be expanded, deleted, or modified. Specifically, the scope completion pulse (about 45 microseconds after the last dpy or dpy-i) interrogates the light pen. If it is seeing light at that time, the light pen status bit and program flag 3 are set. Note that the light does not have to come from the scope face. A threshold control for the light pen is located on the bottom of the scope tube cabinet.

If a program uses dpy-i (iot 7) instructions, there must be at least 45 microseconds between the dpy-i and the time that the status bit (or flag 3) is checked. The light pen status bit gets cleared by any dpy or iot 7. It is read by bit 0 of the status word (see cks instruction). The light pen status bit will cause sequence breaks on channel 5 if it is enabled (see the section on sequence breaks).

Subroutines for tracking the light pen can be found on the "filecase" tape.

3.2.7 Calcomp Plotter

0.005 inch step size
300 steps/sec maximum speed
30 inch by 120 feet maximum paper size
12 inch wide paper adapter
Liquid ink and ball-point pens
5 ink colors
7 liquid ink pen sizes

To use the plotter external level 2 must be assigned. The instruction iot 1111 causes a one-step move as specified by I, which has the following format --

position in I	12	13	14	15	16	17
effect on plotter	up	down	+x	-x	+y	-y

"up" and "down" refer to the pen position.

Continuously moving in the +x direction causes paper to get rolled off of the supply reel onto the floor.

The coordinate system is right-handed.

It is permissable to move simultaneously in one X and one Y direction but not to move in both X or both Y directions. The pen should not be lifted while it is in motion.

The plotter status bit is cleared when an iot 1111 is executed, and is set when the plotter finishes that step. It is read by bit 7 of the status word (see cks instruction). The plotter status bit is on when the plotter is able to be moved again. The plotter status bit will cause sequence breaks on channel 13 if it is enabled.

Subroutines for drawing lines and characters exist in the FORTRAN library.

3.2.8 Buttons and Switches

Four consoles of nine buttons and nine switches each can be added to the PDP-1 to facilitate communications between users and the machine. Two standard panels are available, each of which has a set of buttons and switches on it. Either or both of these may quickly be replaced by inputs from user I/O equipment.

The button and switch states are read into I by the instruction, rbt ("read buttons" = iot x237). This will set a bit in I for each button or switch which is on. Buttons go into I[0-8], and switches into I[9-17]. The x field of the instruction determines which of the four panels is being read.

panel 0 = rbt
panel 1 = rbt 400
panel 2 = rbt 1000
panel 3 = rbt 1400

There is also a way of determining when any button changes. See part 5 of this Instruction Manual.

3.2.9 Knobs

Four consoles of four analog devices each can be added to the computer. Two consoles with four knobs each currently exist.

These may be replaced by inputs from external equipment by simply changing plugs. In the cable is a reference voltage which is nominally -10 volts. When triggered by a ckn instruction, the digital to analog converter measures the ratio of input voltage to reference voltage and puts this fraction in I[10-17]. In the case of the knobs, a reading of zero means the knob is fully counter-clockwise, while 377 means that it is fully clockwise.

The ckn instruction ("check knobs", = iot 27) has the following format --

Bit	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17
	1	1	1	0	1	-	-	-	C	C	K	K	0	1	0	1	1	1

Op.Code 72-iot device 27=knobs

ignored console knob

3.2.11 Music Hardware

The music hardware consists of six identical channels, one per voice. Each channel has a flip-flop which can be loaded from the accumulator sign bit (A[0]) by the appropriate iot instruction. The rate at which this flip-flop is turned on and off determines the pitch of the note played by that voice. The volume level for a given channel is controlled by three bits of the External Register. Zero in these bits is the softest, seven the loudest.

voice	loudness controlled by ext. reg. bits
0	6-8
1	9-11
2	12-15
3	16-18
4	0-2
5	3-5

Instruction	Function
720n14	A[0] to voice n flip-flop, n=0,1,2,3,4,5

A switch associated with each of channels 0-3 determines whether the output of that channel is connected to the left or right inputs of the stereo power amplifier. Voices 4 and 5 are connected to the right side. Four degrees of treble roll-off can be applied to the left and right sides independently. This is controlled by four toggle switches, two per side.

See the Music Programs memo, PDP-43, for information on the music compiler and the music player.

3.2.12 TX-0/PDP-1 Data Link

A parallel 18-bit, two-way data link exists between the TX-0 Live Register and the PDP-1. Data from the PDP-1 to the TX-0 must be sent via the PDP-1 External Register. Data from the TX-0 will go into the External Register if it is assigned. Otherwise, the I register is used.

To use the link facility, external level 1 must be assigned in the PDP-1. The link flip-flop will cause sequence breaks on channel 2 if it is enabled (see the section on sequence breaks).

PDP-1 Instructions

iot 611X	Skip next instruction if the link flip-flop is on
iot 621X	Clear the link flip-flop
iot 631X	Read the TX-0 Live Register into the PDP-1 External Register if it is assigned. Otherwise, into I.

TX-0 Instructions

opr 17000 (ex7)	Set the link flip-flop
opr 1N000 (exN)	Inclusive or the PDP-1 External Register into the TX-0 Live Register.
540000 (tlv)	Test the link flip-flop. This instruction can be made to skip if the link flip-flop is set ("1") or cleared ("0").

The above TX-0 Instructions are governed by the patch panel.

Sending Data from the PDP-1 to the TX-0

Assume that the link flip-flop is set and the TX-0 is in a tlv loop waiting for the link to be cleared. After the PDP-1 has put a word to be sent in the External Register, it clears the link flip-flop and goes into a loop waiting for it to go on again. When the TX-0 sees that the link has been cleared, it comes out of its tlv loop, reads the data word, stores it, and finally sets the link flip-flop. This causes the PDP-1 to come out of its wait loop and signals it that the TX-0 is ready to accept the next word.

Sending Data from the TX-0 to the PDP-1

In this mode, the link Flip-flop is on when the PDP-1 should read a word from the TX-0, and cleared when the TX-0 is getting the next word to be sent.

3.2.13 8-bit D→A Converter

The input to the 8-bit digital to analog converter is bits 10-17 of the External Register. The output will be -10 volts times the fraction in ER[10-17]. The output appears on a BNC connector inside bay 10.

3.2.14 9-bit D→A Converter

External level 3 must be assigned touse the 9-bit D→A converter. The instruction iot x71x loads the input buffer of the converter from I[9-17]. The output will be +10 volts times the fraction in the input buffer. The output appears on a BNC connector inside bay 10.

3.2.15 Clock

The clock is a device which can cause sequence breaks at regular intervals. The time between clock "ticks" is governed by knobs in bay 10. To use the clock, external level 4 must be assigned. The clock status bit is set each time the clock ticks, and is cleared by the instruction iot x61x. The clock status bit will cause sequence breaks on channel 1 if it is enabled. See the section on sequence breaks.

3.3 The Sequence Break System

The Sequence Break or Program Interrupt System provides a convenient means for controlling several I/O devices which are operating simultaneously. For typical devices in which the data rate is relatively slow, interrupts may be considered as a signal to do another data transfer. (Large "blocks" of data are usually transfered directly to memory through the data channel so that instructions must be executed only to start the transfer -- not for each datum.)

In general an interrupt is caused when an I/O device finishes an operation (when it "completes"). This causes the machine's active registers to be stored in memory and an interrupt service routine to be started. This routine must identify which I/O device caused the interrupt, and either restart it or deactivate its channel (so that it will not continue to cause interrupts). After servicing the interrupt, the service routine dismisses back to the program which was interrupted. This entails restoring the active registers of that program, which were stored in memory when the interrupt occurred, and executing a special indirect jump instruction

```
jmp i 1
```

After that, further sequence breaks may occur.

The active registers can be stored and restored by interrupts and dismiss operations in such a way that the interrupted program cannot tell that it was interrupted. It is as if the service routine ran for an instant of time between two instructions.

When a sequence break happens, the hardware automatically does the following:

1) sets SBH (sequence break hold flip-flop) to prevent subsequent breaks.

2) stores A (the accumulator) in location 0.

3) stores G (the program counter, which points back to the next executable instruction in the interrupted program) in location 1. OVF (overflow), EXD (extend mode), and PRV are saved in the top three bits of this word. See memo PDP-35, part 1. OVF and EXD are cleared. The PC is set to 00003.

4) stores I (the in-out register) in location 2.

5) the channel number of the device requiring service is put into A.

6) executes the instruction in location 3, usually a jump to the beginning of the service routine.

The service routine may also store the index register X and the flag word F if it desires. Sequence breaks are suppressed whenever AAL is on, so the service routine need not restore AAL.

The following sequence of instructions can be used to restore registers when the service routine is finished. It will work even if the main program was in base address mode.

```
lxr xr      /saved X
lac 0       /saved A
lio flg     /saved flag word
lpf
spi
jmp .+4     /iam or dam
ril is
spi
aam         /undo bam
lio 2       /saved I
jmp i 1
```

Each I/O device is connected to a separate channel of the break system. Lower numbered channels will break first if more than one device needs service at a given time. Thus, devices needing very accurate service are put on the highest priority channels (lowest numbered). Each channel may be activated and deactivated (i.e., assigned and deassigned) by instructions. The device connected to a particular channel will not cause a sequence break unless that channel is assigned (active). When the service routine is started after an interrupt, the breaking channel number will be in A, allowing the device to be identified easily.

Associated with each iot-operated device is a "status" bit. When a given device has its status bit on (a "1"), that device is capable of being restarted, and it will continually try to cause interrupts until its status bit is cleared. An interrupt will happen for a given device if the following conditions are met:

1) The device's status bit is on
2) The channel to which it is connected is assigned
3) SBH is off -- not currently servicing an interrupt
4) No higher priority channel is requesting a break.
5) The computer is in sequence break mode (SBM=1).
6) AAL and ESI are off
7) The processor is not "locked" (see PDP-35, part 4).

The "status word" contains the status bits of some devices. It is read into I by the cks instruction.

status bit	device
0	light pen
2	type out
3	type in
6	sequence break mode
7	plotter
8	PRL

Note that output devices such as the typewriter are initially capable of accepting a character. Thus, a sequence break will occur as soon as such a channel is activated. Usually, a buffer is maintained and the channel is activated only when an item is inserted in the buffer, and deactivated just before removing the last item for output.

INSTRUCTIONS

Mnemonic	Op.Code	Function
esm	720055	Enter sequence break mode (1→SBM) SBM must be off if PRL is on.
lsm	720054	Leave sequence break mode (0→SBM)
cac	720053	Clear (deassign) all channels
asc mn00	72mn51	Assign channel mn. ($0 \leq mn \leq 17$)
dsc mn00	72mn50	Deassign channel mn.
cbs	720056	Clear break system. Delete any break which is about to happen. Turn off SBH to permit breaks.
hld	770057	Hold subsequent breaks (1→SBH).
cks	770033	(check status) Read the status word into I.
jmp i 1	610001	Dismiss. 0→SBH. Restore OVF and EXD, as well as the extended (15-bit) PC.

SEQUENCE BREAK DEVICE DATA

Device	Position in status word	Channel	ext. level	Status bit cleared by	Status bit set by
type-in	3	6	none	tyi	key struck
type-out	2	7	none	tyo	ready to accept another tyo
clock	none	1	4	iot 610	clock "tick"
TX-0 link	none	2	1	iot 6210	TX-0 opr 17000 (ex7)
plotter	7	13	2	iot 1111	plotter ready
light pen	0	5	none	dpy	light, 45 usec. after dpy.
Radio Astr.	none	1	7	iot xx12, iot xy11	
Radio Astr. Middleton	none	0	6	iot 613	begin pulse